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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yeo, *et al.* Docket No.: TSM03-0555  
Serial No.: 10/628,020 Art Unit: 2811  
Filed: July 25, 2003 Examiner: TBD  
For: Capacitor With Improved Capacitance Density and Method of Manufacture

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Respectfully submitted,

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Legal Assistant

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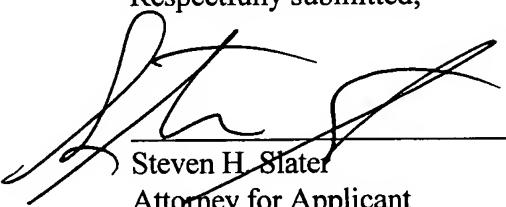
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May 26, 2004

Date

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Respectfully submitted,

  
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Attorney for Applicant  
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Sheet	2	of	5	Application Number	10/628,020
				Filing Date	July 25, 2003
				First Named Inventor	Yeo, et al.
				Art Unit	2811
				Examiner Name	TBD
				Attorney Docket Number	TSM03-0555

## U.S. PATENT DOCUMENTS

Examiner Signature		Date Considered	
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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(use as many sheets as necessary)</i>				Application Number	10/628,020
Sheet	4	of	5	Filing Date	July 25, 2003
				First Named Inventor	Yeo, et al.
				Group Art Unit	2811
				Examiner Name	TBD
				Attorney Docket Number	TSM03-0555

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite, No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T <sup>2</sup>
	45	MATTHEWS, J.W., et al., "Defects in Epitaxial Multilayers – III. Preparation of Almost Perfect Multilayers," Journal of Crystal Growth, Vol. 32, (1976), pp. 265-273.		
	46	SCHÜPPEN, A., et al., "Mesa and Planar SiGe-HBTs on MBE-Wafers," Journal of Materials Science: Materials in Electronics, Vol. 6, (1995), pp. 298-305.		
	47	MATTHEWS, J.W., "Defects Associated with the Accommodation of Misfit Between Crystals," J. Vac. Sci. Technol., Vol. 12, No. 1 (Jan./Feb. 1975), pp. 126-133.		
	48	HUANG, X., et al., "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pp. 880-886.		
	49	SHAHIDI, G.G., "SOI Technology for the GHz Era," IBM J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, pp. 121-131.		
	50	SHIMIZU, A., et al., "Local Mechanical Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," IEDM 2001, pp. 433-436.		
	51	WONG, H.-S.P., "Beyond the Conventional Transistor," IBM J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, pp. 133-167.		
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	54	THOMPSON, S., et al., "A 90 nm Logic Technology Featuring 50nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 um <sup>2</sup> SRAM Cell," IEDM, pp. 61-64.		
	55	WELSER, J., et al., "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," IEDM 1992, pp. 1000-1002.		
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	57	"Future Gate Stack," International Sematech, 2001 Annual Report.		
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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(use as many sheets as necessary)</i>				Application Number	10/628,020
Sheet	3	of	5	Filing Date	July 25, 2003
				First Named Inventor	Yeo, et al.
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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite, No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T <sup>2</sup>
	32	ISMAIL, K., et al., "Electron Transport Properties of Si/SiGe Heterostructures: Measurements and Device Implications," <i>Applied Physics Letters</i> , Vol. 63, No. 5, (August 2, 1993), pp. 660-662.		
	33	NAYAK, D.K., et al., "Enhancement-Mode Quantum-Well Ge <sub>x</sub> Si <sub>1-x</sub> PMOS," <i>IEEE Electron Device Letters</i> , Vol. 12, No. 4, (April 1991), pp. 154-156.		
	34	GÁMIZ, F., et al., "Strained-Si/SiGe-on-Insulator Inversion Layers: The Role of Strained-Si Layer Thickness on Electron Mobility," <i>Applied Physics Letters</i> , Vol. 80, No. 22, (June 3, 2002), pp. 4160-4162.		
	35	GÁMIZ, F., et al., "Electron Transport in Strained Si Inversion Layers Grown on SiGe-on-Insulator Substrates," <i>Journal of Applied Physics</i> , Vol. 92, No. 1, (July 1, 2002), pp. 288-295.		
	36	MIZUNO, T., et al., "Novel SOI p-Channel MOSFETs With Higher Strain in Si Channel Using Double-SiGe Heterostructures," <i>IEEE Transactions on Electron Devices</i> , Vol. 49, No. 1, (January 2002), pp. 7-14.		
	37	TEZUKA, T., et al., "High-Performance Strained Si-on-Insulator MOSFETs by Novel Fabrication Processes Utilizing Ge-Condensation Technique," <i>Symposium On VLSI Technology Digest of Technical Papers</i> , (2002), pp. 96-97.		
	38	JURCZAK, M., et al., "Silicon-on-Nothing (SON) – an Innovative Process for Advanced CMOS," <i>IEEE Transactions on Electron Devices</i> , Vol. 47, No. 11, (November 2000), pp. 2179-2187.		
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	40	MAITI, C.K., et al., "Film Growth and Material Parameters," <i>Application of Silicon-Germanium Heterostructure</i> , Institute of Physics Publishing, Ch. 2 (2001) pp. 32-42.		
	41	TIWARI, S., et al., "Hole Mobility Improvement in Silicon-on-Insulator and Bulk Silicon Transistors Using Local Strain," <i>International Electron Device Meeting</i> , (1997), pp. 939-941.		
	42	OOTSUKA, F., et al., "A Highly Dense, High-Performance 130nm Node CMOS Technology for Large Scale System-on-a-Chip Applications," <i>International Electron Device Meeting</i> , (2000), pp. 575-578.		
	43	MATTHEWS, J.W., et al., "Defects in Epitaxial Multilayers – I. Misfit Dislocations," <i>Journal of Crystal Growth</i> , Vol. 27, (1974), pp. 118-125.		
	44	MATTHEWS, J.W., et al., "Defects in Epitaxial Multilayers – II. Dislocation Pile-Ups, Threading Dislocations, Slip Lines and Cracks," <i>Journal of Crystal Growth</i> , Vol. 29, (1975), pp. 273-280.		
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